WHAT IS CLAIMED IS:

1. – 8. (cancelled)

9. (original) A reconfigurable digital processing system for use in space to permit remote reconfiguration of a space vehicle-born processor, comprising:

a field programmable gate array functioning as a signal processor for performing a signal processing task aboard said space vehicle;

a receiver on said space vehicle for reviewing uploaded commands for reconfiguring said field programmable gate array; and,

a field programmable gate array configuring unit coupled to said receiver for reconfiguring said field programmable gate array responsive to said uploaded commands, whereby a field programmable gate array aboard said space vehicle can be reconfigured from a remote location.

10. (original) The reconfigurable digital processing system of Claim 9, wherein said field programmable gate array includes a testing unit for ascertaining if the operation of said field programmable gate array matches that of a prior configuration, and further including a reconfiguration unit for restoring the priorly configured operation of said field programmable gate array responsive to an output of said testing unit indicating a repairable malfunction of said field programmable gate array.

11. (original) The reconfigurable digital processing system of Claim 9, and further including a number of field programmable gate arrays and a shadowing for providing inputs to each of said gate arrays to permit parallel processing by said field programmable gate arrays.

12. (original) The reconfigurable digital processing system of Claim 9, wherein said field programmable gate array includes a bus and at least one data pipe coupled thereto.

13. (original) The reconfigurable digital processing system of Claim 12, wherein said bus and said data pipe includes a clock coupled thereto.

14. (original) The reconfigurable digital processing system of Claim 9, wherein said field programmable gate array includes a customizable core, an interconnect block coupled to said core, a timing and synchronization unit connected to said interconnect block, an external I/O block coupled to said timing and synchronization unit, the coupling of said interconnect block and said core including at least one data pipe, the coupling of said external I/O block and said timing and synchronization unit including at least one data pipe.

15. (original) The reconfigurable digital processing system of Claim 14, wherein said field programmable gate array includes a common configuration and status unit coupled to said external I/O block and to said core to provide internal interface control thereof.

16. (original) The reconfiguration digital processing system of Claim 15, and further including control logic for providing a time stamp to said configuration and status common configuration and status unit.

17. (original) The reconfigurable digital processing system of Claim 16, and further including at least one bus coupled between said core and said external I/O block, said control logic coupled to said external I/O block for control of the timing of the signals on said bus.

18. (original) The reconfigurable digital processing of Claim 17, and further including a shadow bus control unit coupled between said external I/O block and said common infrastructure configuration and status unit for the control of shadow functions.

19. (original) A reconfigurable digital processing system, comprising:

a card having a number of field programmable gate arrays thereon;

a control unit for controlling the configuration of said field programmable gate arrays;

a configuration bus coupled between said control unit and said field programmable gate arrays;

a bus interface coupled to said field programmable gate arrays; and,

a shadow interconnect between said field programmable gate arrays for connecting said arrays together to perform parallel processing tasks.

20. (original) The system of Claim 19, and further including SRAM storage for said control unit and EEPROM storage for memory and address data from said bus interface.